IN THE CLAIMS

1. (Original) An n-port integrated circuit (IC) switch element, comprising:

n generic ports and an additional generic port to function as a port to an input output processor (IOP), each generic port on the IC switch element including:

an input link to receive data frames from a source off of the IC switch element;

an output link to transmit data frames to a destination off of the IC switch element; and

a steering state machine to direct received data frames from the input link to the output link of one or more of the generic ports on the IC switch element; and

a switch crossbar system to provide an available data channel between each generic port and every other generic port in the IC switch element.

2. (Original) The IC switch element of claim 1, wherein the switch crossbar system includes two or more independent crossbars.

3. (Original) The IC switch element of claim 1, wherein the switch crossbar system includes:

a frame tag crossbar to allow each generic port to send tags to any one or more of the generic ports on the IC switch element;

a frame request crossbar to allow each generic port to send a frame request to any generic port on the IC switch element from which a tag has been received;

a frame status crossbar to allow each generic port to send additional frame information to any one or more of the generic ports on the IC switch element in response to the frame request; and

a status / frame transfer crossbar to allow each generic port to send preconditioning frame status information for proper frame handling and to send a requested frame to any one or more of the generic ports on the IC switch element in response to the frame request.

4. (Original) The IC switch element of claim 1, wherein all of the generic ports on the IC switch element are similar, each generic port including a native identifier to identify a native domain, a native area and a native port for use to steer received data frames.

5. (Original) The IC switch element of claim 1, wherein each generic port on the IC switch element includes circuitry to transfer frames via a frame pull transfer methodology such that a source port sends data frames to a destination port when the destination port requests the data frames to prevent head-of-line blocking.

6. (Original) The IC switch element of claim 1, wherein the steering state machine is adapted to write multiple tags to multiple generic ports on the IC switch element for multicasting data frames to the multiple generic ports.

7. (Original) The IC switch element of claim 1, wherein the steering state machine includes one or more tables, each table having one or more entries, each entry including a valid bit for use to prevent routing of data frames to one or more of the available data channels.

8. (Original) The IC switch element of claim 1, wherein the steering state machine includes an alias cache to store selected addresses for broadcasting and multicasting data frames to multiple generic ports on the IC switch element.

9. (Original) The IC switch element of claim 1, wherein the steering state machine includes a topology identifier to identify a position of the IC switch element in a topology for parsing the received data frame, a domain steering table to identify a chip path to a desired switch domain, an area steering table to identify a chip path to a desired IC switch element in the desired switch domain, and a port steering table to identify a chip path to a desired port in the desired IC switch element and the desired switch domain.

10. (Original) The IC switch element of claim 9, wherein each of the domain steering table, the area steering table and the port steering table have one or more entries, each entry in each table including a valid bit for use in hard zoning to prevent routing of data frames to one or more of the available data channels.

11. (Original) The IC switch element of claim 1, wherein the steering state machine includes:

an alias cache to store selected addresses for broadcasting, multicasting and unicasting data frames to multiple generic ports on the IC switch element; and

one or more tables to identify a chip path for a desired data channel for unicasting data frames to a single generic port on the IC switch element when the received data frames do not match an entry in the alias cache.

12. (Original) The IC switch element of claim 11, wherein:

the alias cache includes a number of alias cache entries to be compared to a destination frame address; and

the alias cache enables selective steering to one or more generic ports within a selected destination based on a comparison of the alias cache entries to at least part of the destination frame address.

13. (Original) The IC switch element of claim 12, wherein the alias cache entries include three bits to enable comparing on Domain ID fields, Area ID fields, and Port ID fields.

14. (Previously Presented) A switch chassis, including:

a number of chassis ports to connect to ports of devices or ports of other switch chassis; and

at least one n-port integrated circuit (IC) switch element, including:

n generic ports and an additional generic port to function as a port to an input output processor (IOP), each generic port on the IC switch element including:

an input link to receive data frames from a source off of the IC switch element;

an output link to transmit data frames to a destination off of the IC switch element; and

a steering state machine to direct received data frames from the input link to the output link of one or more of the generic ports on the IC switch element; and

a switch crossbar system to provide an available data channel between each generic port and every other generic port in the IC switch element,

wherein at least some of the n generic ports are connected to the number of chassis ports

15. (Original) The switch chassis of claim 14, wherein the at least one IC switch element is one n-port switch element, and each of the n generic ports of the IC switch element is connected to one of the chassis ports to form an n-port switch chassis.

16. (Original) The switch chassis of claim 15, wherein the switch chassis is connected to one or more other switch chassis to form a switch network.

17. (Original) The switch chassis of claim 14, wherein:

the at least one IC switch element includes multiple n-port switch elements;

for each of the multiple n-port switch elements, the n generic ports include a first group of generic ports and a second group of generic ports;

the switch chassis further including inter-element links formed between the IC switch elements using the first group of generic ports in the multiple n-port switch elements; and

the switch chassis further including data links to the chassis ports formed using the second group of generic ports.

18. (Original) The switch chassis of claim 17, wherein the inter-element links are configured in a cascade configuration.

19. (Original) The switch chassis of claim 17, wherein the inter-element links are configured in a mesh configuration.

20. (Original) The switch chassis of claim 17, wherein the switch chassis is connected to one or more other switch chassis to form a switch network.

21. (Original) The switch chassis of claim 14, wherein

the at least one IC switch element includes a first group of n-port switch elements and a second group of n-port switch elements;

for each of the first group of n-port switch elements, the n generic ports include a first group of generic ports and a second group of generic ports;

the switch chassis further including inter-element links formed between the first group of generic ports in the first group of IC n-port switch elements and the generic ports in the second group of n-port switch elements; and

the switch chassis further including data links formed between the chassis ports and the second group of generic ports in the first group of n-port switch elements.

22. (Original) The switch chassis of claim 21, wherein:

for each of the first group of IC switch elements, the n generic ports further include a third group of generic ports; and

the switch chassis further includes cascade inter-element links formed between individual elements in the first group of IC switch elements using the third group of generic ports in the first group of IC switch elements.

23. (Original) The switch chassis of claim 21, wherein the switch chassis is connected to one or more other switch chassis to form a switch network.

24. (Original) The switch chassis of claim 14, wherein the switch crossbar system includes two or more independent crossbars.

25. (Original) The switch chassis of claim 24, wherein the switch crossbar system includes:

a frame tag crossbar to allow each generic port to send tags to any one or more of the generic ports on the IC switch element;

a frame request crossbar to allow each generic port to send a frame request to any generic port on the IC switch element from which a tag has been received;

a frame status crossbar to allow each generic port to send additional frame information to any one or more of the generic ports on the IC switch element in response to the frame request; and

a status / frame transfer crossbar to allow each generic port to send preconditioning frame status information for proper frame handling and to send a requested frame to any one or more of the generic ports on the IC switch element in response to the frame request.